REMARKS

Applicants have reviewed the Office Action mailed March 26, 2007. After entry of this amendment, claims 1-4 and 6-12 are pending. Claim 5 has been cancelled without prejudice or disclaimer of the subject matter therein, and claims 13-20 are withdrawn.

CLAIM OBJECTIONS

Applicants are grateful to the Examiner for pointing out the informalities which are now corrected by the above amendments. Applicants have also amended the claims solely to correct additional informalities.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1-4 and 6-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,914,522 to Aiello et al. (Aiello) in view of U.S. Patent Publication No. 2003/0213605 to Brendel et al. (Brendel). Aiello is directed to VIPower technology. The device is made from a chip of N-type semiconductor material comprising a bipolar or field-effect vertical power transistor. The power transistor has a collector or drain region in the N-type material. The semiconductor structure also comprises a PNP bipolar lateral power transistor having a base region in the N-type material in common with the collector or drain region of the vertical power transistor.

Claim 1 is directed to an implantable medical device that includes "a semiconductor substrate; an epitaxial layer overlying the semiconductor substrate; a power transistor formed in the epitaxial layer having a first electrode, a control electrode, and a second electrode wherein a breakdown voltage of the power transistor is greater than 100 volts and wherein current flow of the transistor is vertical through the epitaxial layer to the semiconductor substrate; a backside contact coupling to the first electrode of the power transistor, at least one deep trench etched through the epitaxial layer exposing the semiconductor substrate wherein the at least one deep trench is etched in an area outside a high voltage termination region; and a first electrode contact region coupling to the semiconductor substrate exposed by the at least one deep trench, the first electrode contact region overlying the epitaxial layer."

Regarding claim 1, the Examiner concedes that Aiello does not disclose, teach, or suggest the "deep trench" as claimed and instead asserts that Brendel teaches this element, making the claimed subject matter unpatentable in view of Brendel. Applicants created their invention before Brendel. Applicants submit new affidavits to antedate the publication date of Brendel. The attached affidavits show Applicants' invention date before the filing date of Brendel (February 27, 2003), and further, before any potential priority claim to U.S. Provisional Application No. 60/360,642, filed on February 28, 2002. Accordingly, Brendel is not prior art against Applicants' claims. Further, Aiello does not disclose the deep trench as the Examiner conceded, and it would not have been obvious to one of ordinary skill in the art to modify Aiello to include the deep trench as claimed. Accordingly, Applicants believe claim 1 to be in condition for allowance and respectfully request the rejection of claim 1 be withdrawn. Claims 2-4 and 6-12 are dependent upon claim 1 and are believed to be patentable for at least the same reasons.

In addition, Applicants respectfully assert that the Examiner has not met his burden of establishing a motivation to combine references. Particularly regarding claim 1, Applicants assert that the Examiner used Applicants' claims as a blue print and then merely used a limitation-by-limitation reference-by reference analysis to establish its obviousness rejection. One of skill in the art considering the drawbacks of conventional PNP lateral power transistors addressed in Aiello would not logically consider the EMI feedthrough filter terminals described in Brendel. Accordingly, the rejection of claim 1, and claims 2-4 and 6-12 depending therefrom should be withdrawn.

Further regarding claim 2, Applicants respectfully submit that the Examiner has not shown all the elements in the cited references. Claim 2 includes, *inter alia*, "a plurality of transistor cells formed in the active area region wherein the power transistor comprises the plurality of transistor cells coupled in parallel." Applicants assume the Examiner asserts that this limitation is shown in Figures 2a and 3 of Aiello. Applicants respectfully submit that Figures 2a and 3 show an NPN transistor and a PNP transistor, but not in parallel. As Aiello illustrates, the collector of the NPN transistor is coupled with the base of the PNP transistor. As such, the transistors are not in parallel. Thus Aiello does not show all the elements of claim 2. Applicants believe claim 2 to be in

condition for allowance for at least this additional reason and respectfully request the rejection of claim 2, and claims 3-4 and 6-12 depending therefrom be withdrawn.

Applicants respectfully assert that claim 1 and claims 2-4 and 6-12 depending therefrom are in condition for allowance. Withdrawal of the instant rejections and issuance of a Notice of Allowance is respectfully requested.

Respectfully submitted,

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Date

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